Optimized Hybrid Phase Disposition PWM Control Method for Multilevel Inverter

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Abstract—This paper presents a new variation of hybrid phase disposition pulse width modulation technique suitable for cascaded multilevel inverter. A hybrid PDPWM is developed based on low frequency PWM and high frequency Sinusoidal PWM. An optimized sequential switching scheme introduced in this proposed method to equalize electro static and electro magnetic stress among the power devices. It is confirmed that the proposed technique offers significantly lower switching losses and switching transitions. Furthermore, the proposed hybrid PDPWM offers better harmonic performance compared to its conventional PWM counterpart. Simulation results are included in this paper in order to confirm the effectiveness of the proposed technique.

***Keywords*-Pulse width modulation, phase disposition pulse width modulation, hybrid phase disposition pulse width modulation, cascaded multilevel inverter.**

I. INTRODUCTION

Multilevel inverter is an effective solution for increasing power and reducing harmonics of ac waveforms. A multilevel inverter has four main advantages over the conventional bipolar inverter. First, the voltage stress on each switch is decreased due to series connection of the switches. Therefore, the rated voltage and consequently the total power of the inverter could be safely increased. Second, the rate of change of voltage (dv/dt) is decreased due to the lower voltage swing of each switching cycle. Third, harmonic distortion is reduced due to more output levels. Forth, lower acoustic noise and electromagnetic interference (EMI) is obtained [1].

Based on these advantages, various circuit topologies and modulation strategies have been reported for better utilization of multilevel voltage source inverters. Multilevel topologies are classified in to three categories: diode clamped inverters, flying capacitor inverters and cascaded inverters. The topologies have an equal number of main switches [2]-[3]. The diode clamped inverter uses a single dc bus that is subdivided in to number of voltage levels by a series string of capacitors. A matrix of semiconductor switches and diodes allows each phase leg output to be switched to any of these voltage levels. The main drawback of diode clamped inverter is the unbalanced dc link capacitor. It restricts the application of diode clamped inverter to five or less number of levels. Flying capacitor inverter requires the most number of capacitors. Cascaded inverter has simple structure but it needs various separate dc sources. A particular advantage of this topology is that the modulation, control and protection requirements of each bridge are modular. The complexity has generally restricted cascaded inverters to the higher power range where several switched output voltage levels are needed and diode clamped structure is unsuitable because of the difficulty of balancing the series dc capacitor voltages [4].

Modulation control of any type of multilevel inverter is quite challenging, and much of the reported research is based on somewhat heuristic investigations. Multilevel inverter systems have been compared on the basis of overall performance, with little attempt being made to adapt the best modulation strategy for one topology to other structures. In this paper, cascaded multilevel inverter topology as shown in fig.1 used to investigate the proposed hybrid phase disposition PWM control scheme. The proposed method can be equally applied to any number of levels.

II. CONVENTIONAL CARRIER BASED MODULATION SCHEMES

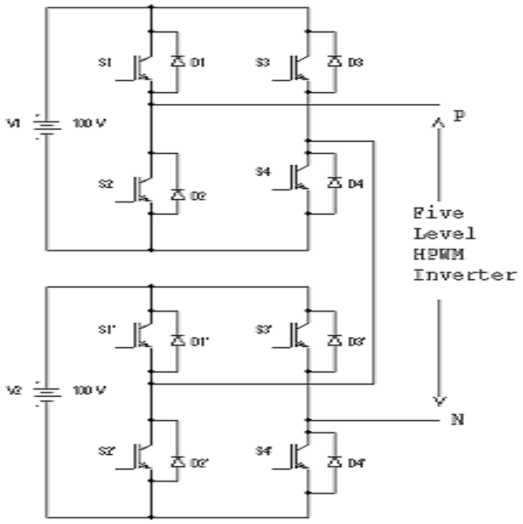

Fig.1. Schematic diagram of the inverter topology used to verify the proposed five level (line to neutral) HPDPWM method

Multilevel pulse width modulation is based on comparison of sinusoidal reference signal with each carrier to determine the voltage level that the inverter

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should switch to. Carrier based N level PWM operation consists of N-1 different carriers [5]. The carriers have the same frequency f_c, the same peak to peak amplitude V, and are disposed so that the bands they occupy are contiguous. They are defined as

$$C_i = V((-1)^{f(i)}\, y_c(\omega_c, \varphi) + i - \frac{N}{2}),\ i = 1,..., N-1$$

where y_c is a normalized symmetrical triangular carrier defined as

$$y_c(\omega_c, \varphi) = (-1)^{[\alpha]}((\alpha \bmod 2) - 1) + \frac{1}{2},$$

$$\alpha = \frac{\omega_c t + \varphi}{\pi}, \omega_c = 2\pi f_c$$

φ represents the phase angle of y_c. y_c is a periodic function with the period $T_c = 2\pi / \omega_c$ .It is shown that using symmetrical triangular carrier generates less harmonic distortion at the inverter's output [6].

Three alternative carrier disposition PWM strategies are commonly referenced, viz:

(i) alternative phase opposition disposition (APOD), where each carrier is phase shifted by π from its adjacent carrier;

(ii) phase opposition disposition (POD), where the carriers above the sinusoidal reference zero point are π out of phase with those below the zero point;

(iii) phase disposition (PD), where all carriers are in phase. It is generally accepted that the PD strategy gives rise to the lowest harmonic distortion for the line to line voltage [7].

While the multilevel PWM techniques developed thus far have been extensions of two level PWM methods, the multiple levels in a cascaded inverter offer extra degrees of freedom and greater possibilities in terms of device utilization, state redundancies, and effective switching frequency. In this paper, novel hybrid multilevel PWM scheme is presented which take advantage of the special properties available in conventional PWM methods and to minimize switching losses with better harmonic performance. Fig.2. shows the carriers and the reference signals for a five level PWM using PD technique with mi=0.8 and carrier frequency f_c =1050 hz.

III. PROPOSED HYBRID PWM CONTROL METHOD

The proposed hybrid PWM is the combination of low frequency PWM and high frequency SPWM. In each cell of cascaded inverter, the four power devices are operated

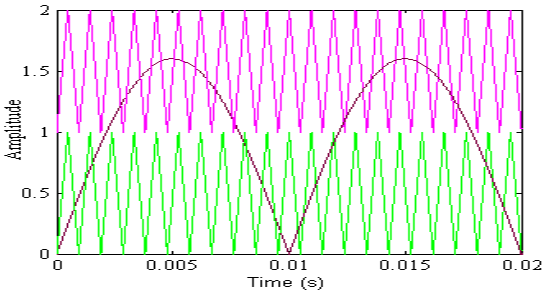

Fig.2.Reference and Carrier Signals for a five level inverter

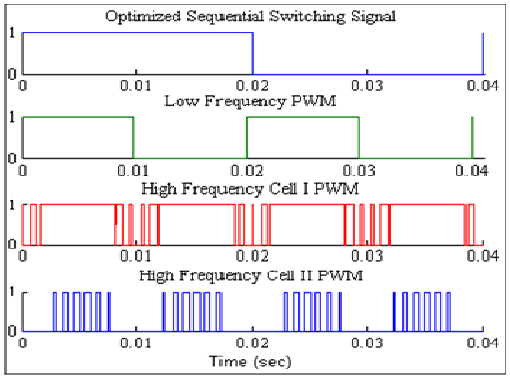

Fig.3. Low and High frequency PDPWM pulses at mi=0.8 and fc=1050 hz

at two different frequencies, two being commutated at low frequency, i.e., the fundamental frequency of the output, while the other two power devices are pulse width modulated at high frequency. This arrangement causes the problem of differential switching losses among the switches.

An optimized sequential signal added to the hybrid PWM pulses to overcome this problem. The low and high frequency PWM signal are shown in fig.3. An optimized hybrid PDPWM method commutates the power switches at high frequency and low frequency sequentially. A common sequential signal and low frequency PWM signals are used for all cells in cascaded inverter. A high frequency SPWM for each cell is obtained by the comparison of the rectified modulation waveform with corresponding phase disposition carrier signal. The low frequency PWM signal should be synchronized with the modulation waveform. In fig.4, the gate pulses are generated by a hybrid PWM controller. This controller is designed to mix the sequential signal, low frequency PWM and high frequency phase disposition sinusoidal PWM and to generate the appropriate gate pulses for cascaded inverter.

IV. GENERALIZATION OF THE PROPOSED HYBRID PWM TECHNIQUE

The previous section has presented the formulation of an optimized hybrid PDPWM switching pattern of a five level inverter. For completeness, the generalized formulation that suits N level inverter is presented.

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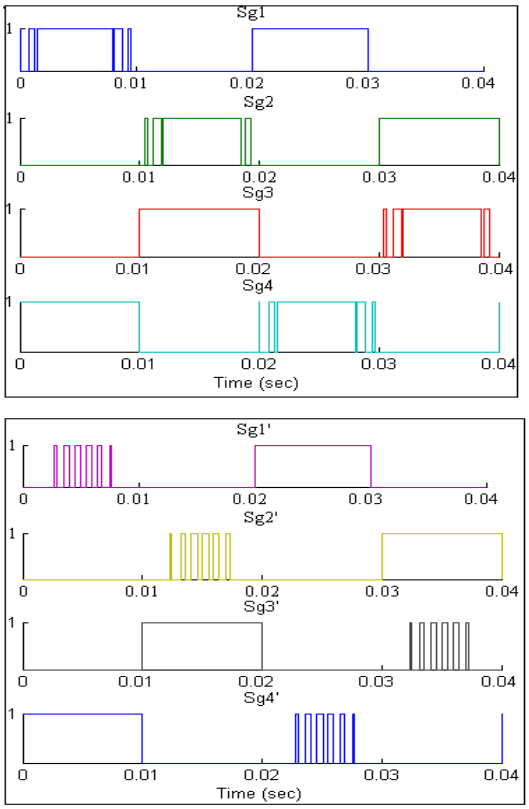


Fig.4. Optimized Hybrid PDPWM switching pattern for five level cascaded multilevel inverter

Let N be the number of levels of the cascaded inverter. M is the number of inverter cells, M=N-1/2. The modulation index is therefore defined as mi= A_m / MA_c and the definition of the frequency ratio mf= f_c / f_m, where f_c as carrier frequency and f_m as modulating signal frequency. The modulating signal A_m is modified based on number of levels and modulation index.

A modified sinusoidal modulating signal is then compared with each phase disposition carrier signal separately to generate M number of high frequency sinusoidal PWM signals. A hybrid PWM controller is used to mix low frequency PWM and the corresponding high frequency SPWM for M^{th} inverter cell. This hybrid PWM for M^{th} inverter cell is then optimized with sequential signal in order to equalize switching transitions. Similarly, hybrid PWM pulses are developed for all cells in any level cascaded inverter.

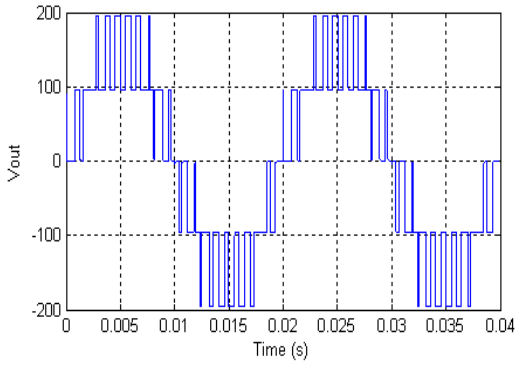
V. RESULTS AND DISCUSSION

A five level cascaded multilevel inverter model was built in MATLAB/Simulink software to demonstrate the feasibility of the hybrid PDPWM and for comparison with conventional PDPWM technique. Fig.5. (a) and (b) shows the output phase and line voltage waveforms with its harmonic spectrum at f_c=1050 hz, f_m=50 hz and mi=0.8 for a five level inverter. For justifiable comparison, a performance index namely total harmonic distortion (THD) was chosen to evaluate both techniques and plotted in fig.10. The THD is calculated using (1) and up to 50th order of harmonics is taken in to account. The low pass filter and the nature of the highly inductive load will take care of the higher order of harmonics.

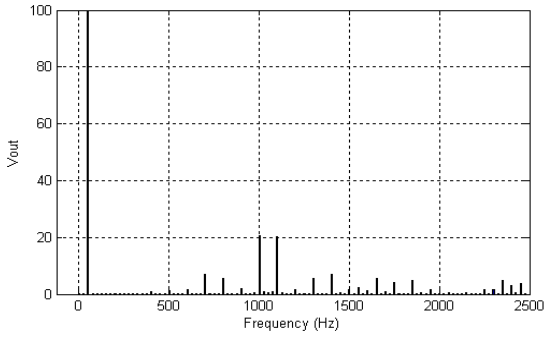
$$THD = \frac{\sqrt{\sum_{n=2}^{50} V_n^2}}{V_1} \qquad (1)$$

The most accurate method of determining switching losses is to plot the current and voltage waveform in the power switch during switching transition and multiplies the waveform point by point to get an instantaneous power waveform. The area under the power waveform is the switching energy at turn on or turn off [8]. In this paper, the average switching losses are calculated based on the information of the data sheet, turn on energy losses per pulse (Eon), turn off energy losses per pulse (Eoff) including reverse recovery loss and switching frequency $f_s = 1/T_s$.

$$P_{sw} = \frac{1}{2\pi T_s} \Sigma(Eon + Eoff) \qquad (2)$$



(a)



(b)

Fig.5 (a).Line to neutral output voltage waveform at mi=0.8 and fc=1050 hz. (b).Harmonic Spectrum of the line to neutral output voltage.

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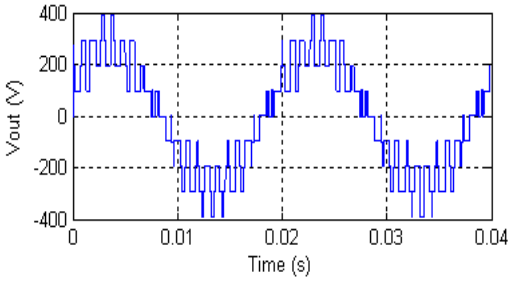
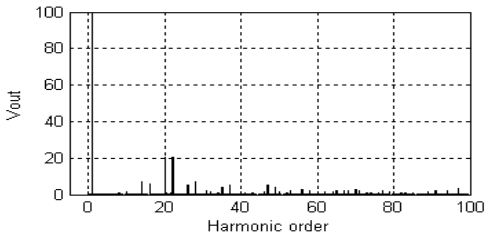


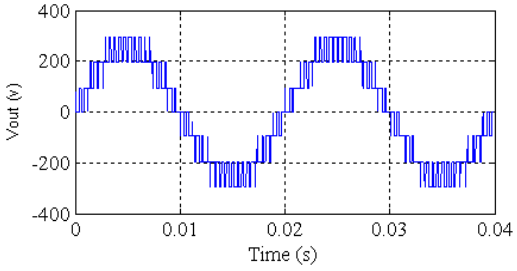
(a)



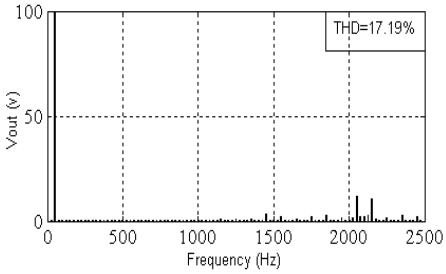
(b)

Fig.6 (a).Line to line output voltage waveform at mi=0.8 and fc=1050 hz. (b).Harmonic Spectrurm of the line to line output voltage.

The proposed hybrid PDPWM scheme is also implemented in seven, nine, eleven level cascaded inverter and the results are provided. It is obviously found that the proposed hybrid PWM offers lower THD compared to conventional PWM one, thus the superiority. Furthermore, it is also noticed that the higher the value of modulation index lower the THD. This method reduces the switching losses up to 42 % and equalizes the switching losses among the power switches in each inverter cell.

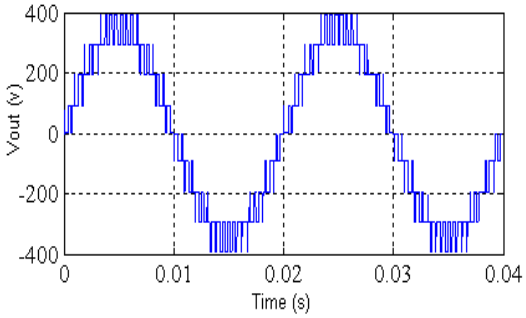


(a)

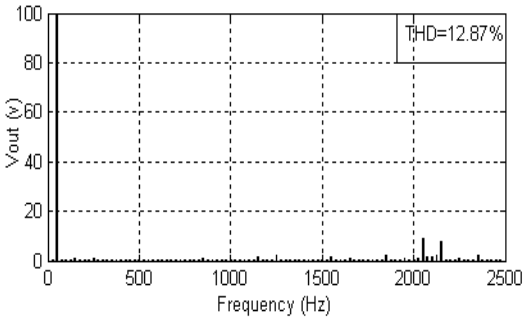


(b)

Fig.7 (a).Line to neutral output voltage waveform for a seven level inverter at mi=0.9 and fc=2100 hz and (b). Harmonic Spectrurm of the line to neutral output voltage.

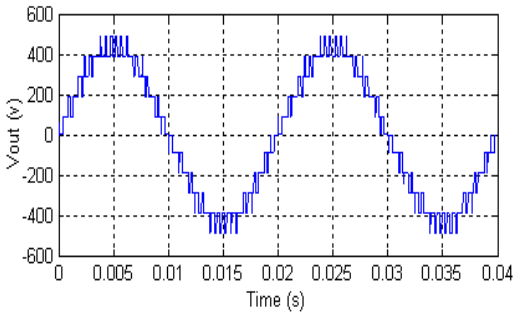


(a)

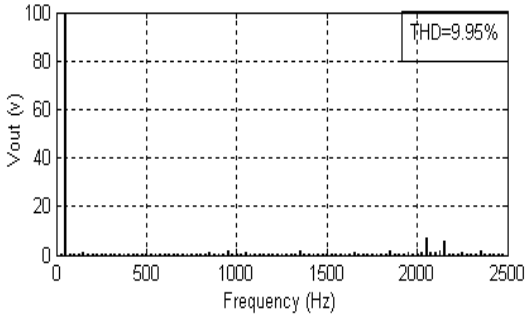


(b)

Fig.8 (a).Line to neutral output voltage waveform for a nine level inverter at mi=0.9 and fc=2100 hz. (b).Harmonic Spectrurm of the line to neutral output voltage.



(a)



(b)

Fig.9 (a).Line to neutral output voltage waveform for a eleven level inverter at mi=0.9 and fc=2100 hz. (b).Harmonic Spectrurm of the line to neutral output voltage

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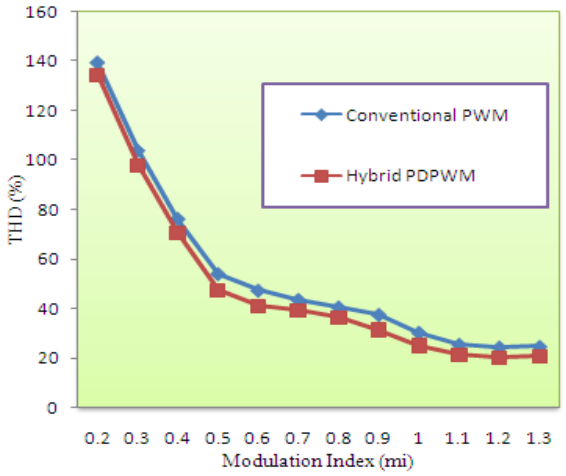

Fig.10.THD vs.Modulation index for five level inverter at fc=1050 hz

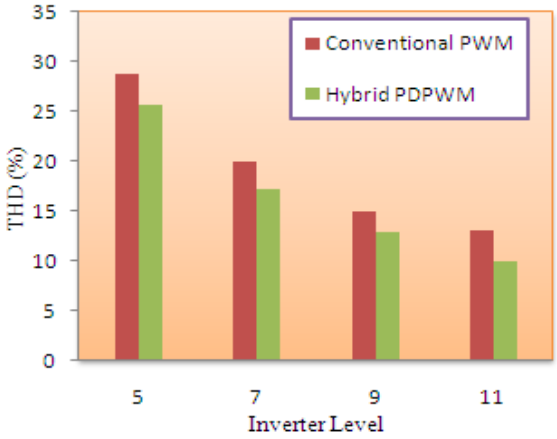

Fig.11.THD comparision for general cascaded multilevel inverter at mi=0.9 and fc=1050 hz

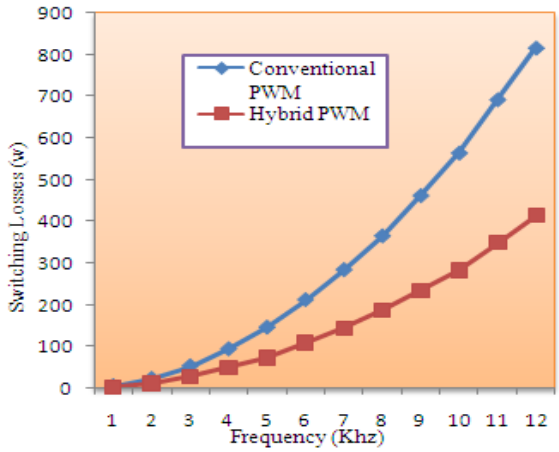

Fig.12. Switching Loss comparision for cascaded multilevel inverter at mi=0.8 .

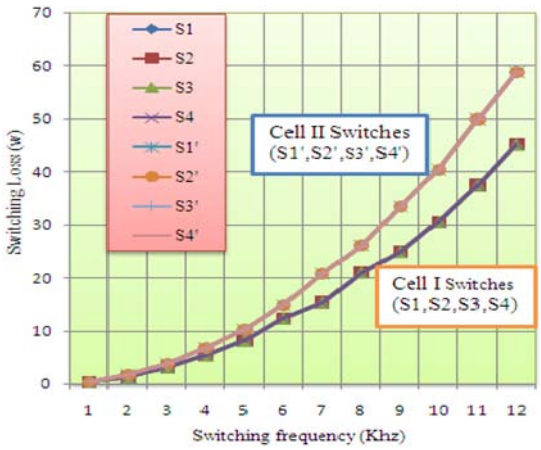

Fig.13. Switching loss analysis among the power switches in a cascaded multilevel inverter at mi=0.8 .

VI. CONCLUSION

An optimized hybrid phase disposition PWM control scheme for cascaded multilevel inverter is proposed in this paper. A hybrid PDPWM controller is designed to generate optimum gate pulses for power switches. When compared with the conventional PWM technique, the proposed method offers lower switching losses throughout the entire range of the switching frequency. Voltage and current stress of power switches in each cell of cascaded inverter are equalized. Furthermore, the proposed hybrid PDPWM offers better harmonic performance compared to its conventional PWM counterpart. Simulation results are also included for several multilevel inverters using hybrid PDPWM control method.

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